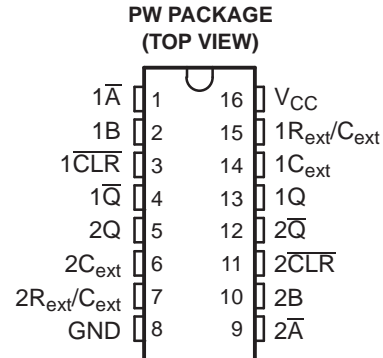


DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH SCHMITT-TRIGGER INPUTS

FEATURES

- Qualified for Automotive Applications
 - Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
 - Typical V_{OHV} (Output V_{OH} Undershoot) >2.3 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
 - Supports Mixed-Mode Voltage Operation on All Ports
 - Schmitt-Trigger Circuitry on \overline{A} , B, and \overline{CLR} Inputs for Slow Input Transition Rates
 - Edge Triggered From Active-High or Active-Low Gated Logic Inputs
 - I_{off} Supports Partial-Power-Down Mode Operation
 - Retriggerable for Very Long Output Pulses, up to 100% Duty Cycle
 - Overriding Clear Terminates Output Pulse
 - Glitch-Free Power-Up Reset on Outputs
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)



DESCRIPTION/ORDERING INFORMATION

The SN74LV123A is a dual retriggerable monostable multivibrator designed for 2-V to 5.5-V V_{CC} operation.

This edge-triggered multivibrator features output pulse-duration control by three methods. In the first method, the \overline{A} input is low, and the B input goes high. In the second method, the B input is high, and the \overline{A} input goes low. In the third method, the \overline{A} input is low, the B input is high, and the clear (\overline{CLR}) input goes high.

The output pulse duration is programmable by selecting external resistance and capacitance values. The external timing capacitor must be connected between C_{ext} and R_{ext}/C_{ext} (positive) and an external resistor connected between R_{ext}/C_{ext} and V_{CC} . To obtain variable pulse durations, connect an external variable resistance between R_{ext}/C_{ext} and V_{CC} . The output pulse duration also can be reduced by taking \overline{CLR} low.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. The \overline{A} , B, and \overline{CLR} inputs have Schmitt triggers with sufficient hysteresis to handle slow input transition rates with jitter-free triggering at the outputs.

Once triggered, the basic pulse duration can be extended by retriggering the gated low-level-active (\overline{A}) or high-level-active (B) input. Pulse duration can be reduced by taking \overline{CLR} low. The input/output timing diagram illustrates pulse control by retriggering the inputs and early clearing.

During power up, Q outputs are in the low state, and \overline{Q} outputs are in the high state. The outputs are glitch free, without applying a reset pulse.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ORDERING INFORMATION⁽¹⁾

T _A	PACKAGE ⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 105°C	TSSOP – PW	Tape and reel	SN74LV123ATPWRQ1	LV123AQ

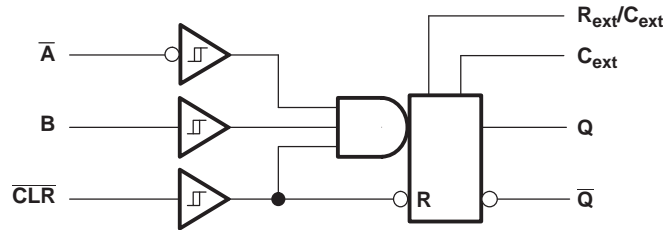
- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

**FUNCTION TABLE
(EACH MULTIVIBRATOR)**

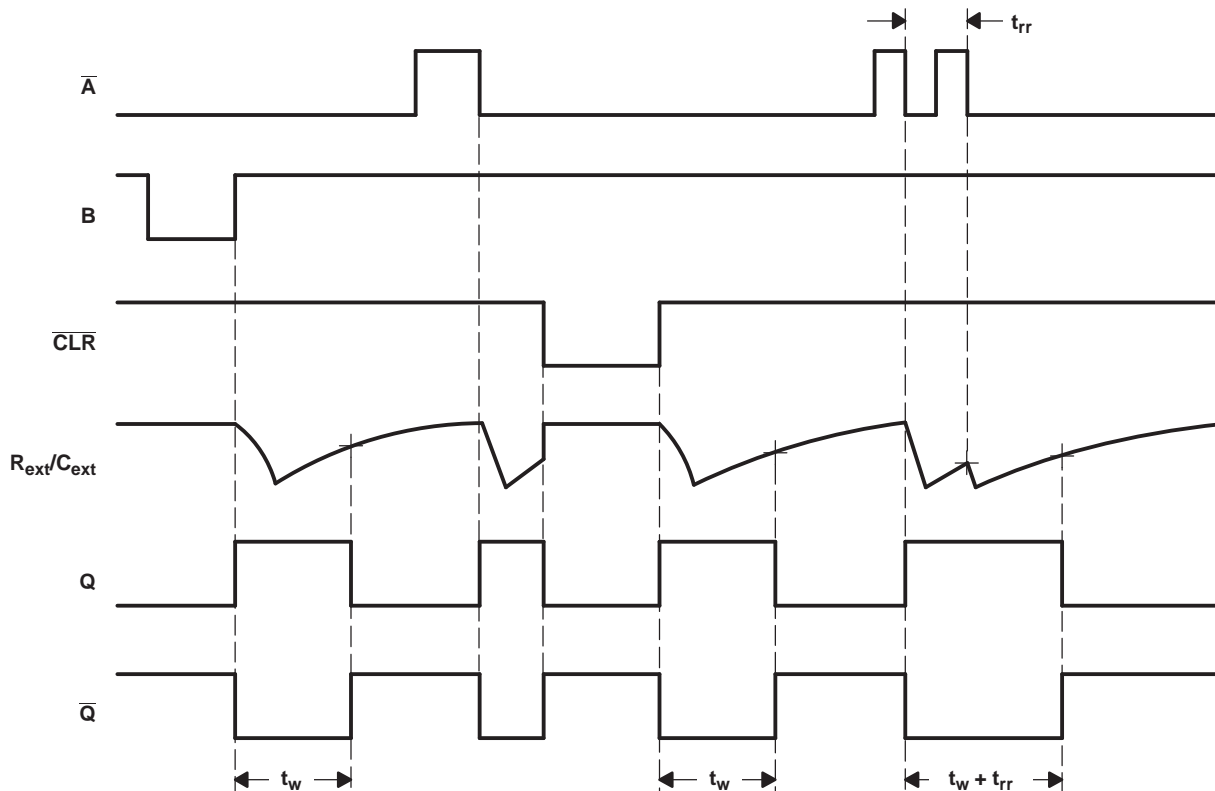
INPUTS			OUTPUTS	
CLR	\bar{A}	B	Q	\bar{Q}
L	X	X	L	H
X	H	X	L ⁽¹⁾	H ⁽¹⁾
X	X	L	L ⁽¹⁾	H ⁽¹⁾
H	L	↑	⌋	⌌
H	↓	H	⌋	⌌
↑	L	H	⌋	⌌

- (1) These outputs are based on the assumption that the indicated steady-state conditions at the A and B inputs have been set up long enough to complete any pulse started before the setup.

LOGIC DIAGRAM, EACH MULTIVIBRATOR (POSITIVE LOGIC)



INPUT/OUTPUT TIMING DIAGRAM



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	-0.5	7	V
V_I	Input voltage range ⁽²⁾	-0.5	7	V
V_O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	-0.5	7	V
V_O	Output voltage range in the high or low state ⁽²⁾⁽³⁾	-0.5	$V_{CC} + 0.5$	V
V_O	Output voltage range in power-off state ⁽²⁾	-0.5	7	V
I_{IK}	Input clamp current	$V_I < 0$	-20	mA
I_{OK}	Output clamp current	$V_O < 0$	-50	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}	±25	mA
	Continuous current through V_{CC} or GND		±50	mA
θ_{JA}	Package thermal impedance ⁽⁴⁾		113	C/W
T_{stg}	Storage temperature range	-65	150	C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) The value is limited to 5.5 V maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 2$ V	1.5	V
		$V_{CC} = 2.3$ V to 2.7 V	$V_{CC} \times 0.7$	
		$V_{CC} = 3$ V to 3.6 V	$V_{CC} \times 0.7$	
		$V_{CC} = 4.5$ V to 5.5 V	$V_{CC} \times 0.7$	
V_{IL}	Low-level input voltage	$V_{CC} = 2$ V	0.5	V
		$V_{CC} = 2.3$ V to 2.7 V	$V_{CC} \times 0.3$	
		$V_{CC} = 3$ V to 3.6 V	$V_{CC} \times 0.3$	
		$V_{CC} = 4.5$ V to 5.5 V	$V_{CC} \times 0.3$	
V_I	Input voltage	0	5.5	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2$ V	-50	μA
		$V_{CC} = 2.3$ V to 2.7 V	-2	mA
		$V_{CC} = 3$ V to 3.6 V	-6	
		$V_{CC} = 4.5$ V to 5.5 V	-12	
I_{OL}	Low-level output current	$V_{CC} = 2$ V	50	μA
		$V_{CC} = 2.3$ V to 2.7 V	2	mA
		$V_{CC} = 3$ V to 3.6 V	6	
		$V_{CC} = 4.5$ V to 5.5 V	12	
R_{ext}	External timing resistance	$V_{CC} = 2$ V	5	kΩ
		$V_{CC} \geq 3$ V	1	
C_{ext}	External timing capacitance	No restriction		pF
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	1		ms/V
T_A	Operating free-air temperature	-40	105	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
V _{OH}		I _{OH} = -50 μA	2 V to 5.5 V	V _{CC} - 0.1			V
		I _{OH} = -2 mA	2.3 V	2			
		I _{OH} = -6 mA	3 V	2.48			
		I _{OH} = -12 mA	4.5 V	3.8			
V _{OL}		I _{OL} = 50 μA	2 V to 5.5 V			0.1	V
		I _{OL} = 2 mA	2.3 V			0.4	
		I _{OL} = 6 mA	3 V			0.44	
		I _{OL} = 12 mA	4.5 V			0.55	
I _I	R _{ext} /C _{ext} ⁽¹⁾	V _I = 5.5 V or GND	5.5 V			±2.5	μA
	\overline{A} , B, and \overline{CLR}	V _I = 5.5 V or GND	0 V			±1	
			0 to 5.5 V			±1	
I _{CC}	Quiescent	V _I = V _{CC} or GND, I _O = 0	5.5 V			20	μA
I _{CC}	Active state (per circuit)	V _I = V _{CC} or GND, R _{ext} /C _{ext} = 0.5 V _{CC}	3 V			280	μA
			4.5 V			650	
			5.5 V			975	
I _{off}		V _I or V _O = 0 to 5.5 V	0 V			5	μA
C _i		V _I = V _{CC} or GND	3.3 V			1.9	pF
			5 V			1.9	

(1) This test is performed with the terminal in the off-state condition.

Timing Requirements

 over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see [Figure 1](#))

PARAMETER		TEST CONDITIONS		T _A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t _w	Pulse duration	\overline{CLR}					5		ns
		\overline{A} or B trigger					5		
t _{rr}	Pulse retrigger time	R _{ext} = 1 kΩ	C _{ext} = 100 pF	(1)	76		(1)		ns
			C _{ext} = 0.01 μF	(1)	1.8		(1)		μs

 (1) See retriggering data in the *application information* section

Timing Requirements

 over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see [Figure 1](#))

PARAMETER		TEST CONDITIONS		T _A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t _w	Pulse duration	\overline{CLR}					5		ns
		\overline{A} or B trigger					5		
t _{rr}	Pulse retrigger time	R _{ext} = 1 kΩ	C _{ext} = 100 pF	(1)	59		(1)		ns
			C _{ext} = 0.01 μF	(1)	1.5		(1)		μs

 (1) See retriggering data in the *application information* section

Switching Characteristics

over recommended operating free-air temperature range, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{pd}	\bar{A} or B	Q or \bar{Q}	$C_L = 50 \text{ pF}$	11.8	24.1		1	27.5	ns
	$\overline{\text{CLR}}$	Q or \bar{Q}		10.5	19.3		1	22	
	$\overline{\text{CLR}}$ trigger	Q or \bar{Q}		12.3	25.9		1	29.5	
$t_w^{(1)}$		Q or \bar{Q}	$C_L = 50 \text{ pF}$ $C_{ext} = 28 \text{ pF}$ $R_{ext} = 2 \text{ k}\Omega$	182	240		300	ns	
			$C_L = 50 \text{ pF}$ $C_{ext} = 0.01 \mu\text{F}$ $R_{ext} = 10 \text{ k}\Omega$	90	100	110	90	110	μs
			$C_L = 50 \text{ pF}$ $C_{ext} = 0.1 \mu\text{F}$ $R_{ext} = 10 \text{ k}\Omega$	0.9	1	1.1	0.9	1.1	ms
$\Delta t_w^{(2)}$			$C_L = 50 \text{ pF}$	± 1				%	

(1) t_w = Duration of pulse at Q and \bar{Q} outputs

(2) Δt_w = Output pulse-duration variation (Q and \bar{Q}) between circuits in same package

Switching Characteristics

over recommended operating free-air temperature range, $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{pd}	\bar{A} or B	Q or \bar{Q}	$C_L = 50 \text{ pF}$	8.3	14		1	16	ns
	$\overline{\text{CLR}}$	Q or \bar{Q}		7.4	11.4		1	13	
	$\overline{\text{CLR}}$ trigger	Q or \bar{Q}		8.7	14.9		1	17	
$t_w^{(1)}$		Q or \bar{Q}	$C_L = 50 \text{ pF}$ $C_{ext} = 28 \text{ pF}$ $R_{ext} = 2 \text{ k}\Omega$	167	200		240	ns	
			$C_L = 50 \text{ pF}$ $C_{ext} = 0.01 \mu\text{F}$ $R_{ext} = 10 \text{ k}\Omega$	90	100	110	90	110	μs
			$C_L = 50 \text{ pF}$ $C_{ext} = 0.1 \mu\text{F}$ $R_{ext} = 10 \text{ k}\Omega$	0.9	1	1.1	0.9	1.1	ms
$\Delta t_w^{(2)}$			$C_L = 50 \text{ pF}$	± 1				%	

(1) t_w = Duration of pulse at Q and \bar{Q} outputs

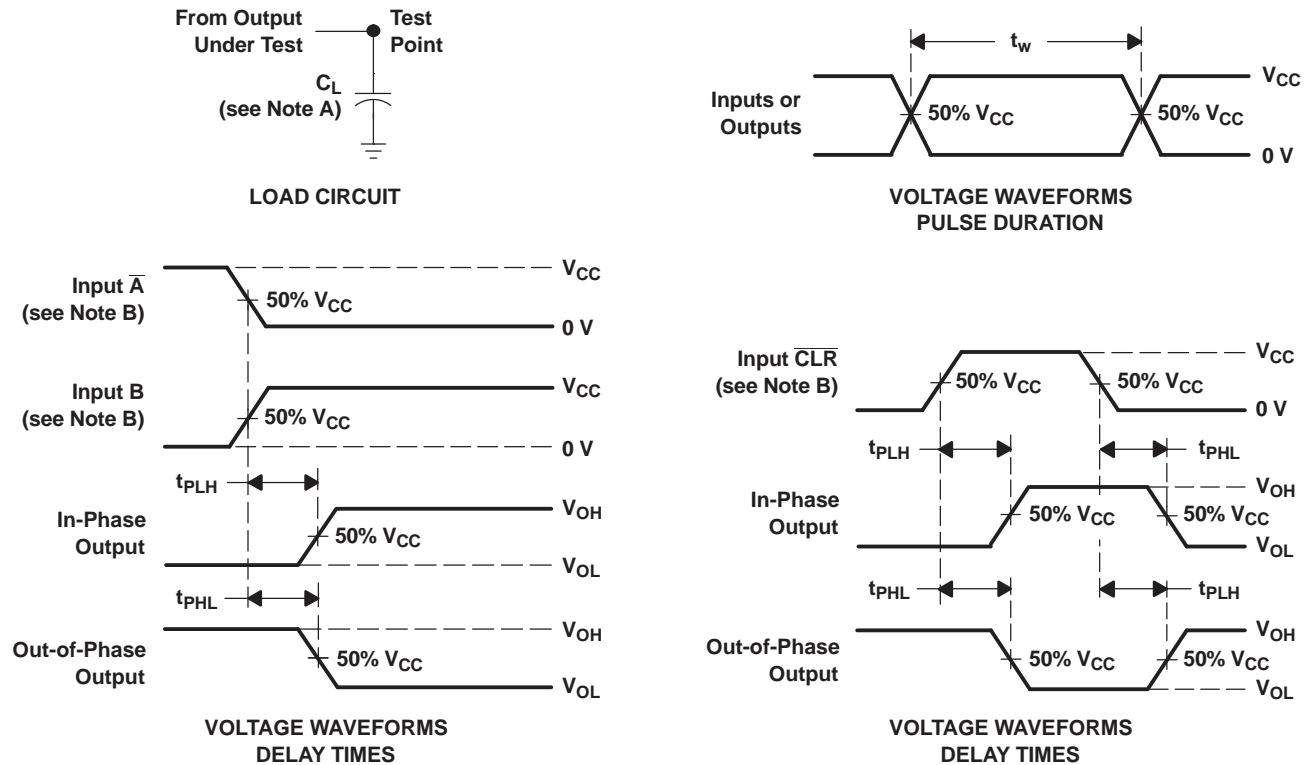
(2) Δt_w = Output pulse-duration variation (Q and \bar{Q}) between circuits in same package

Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	$C_L = 50 \text{ pF}$,	$f = 10 \text{ MHz}$	3.3 V	44	pF
				5 V	49	

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O = 50 \Omega$, $t_r = 3$ ns, $t_f = 3$ ns.
 C. The outputs are measured one at a time, with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

APPLICATION INFORMATION

Operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied.

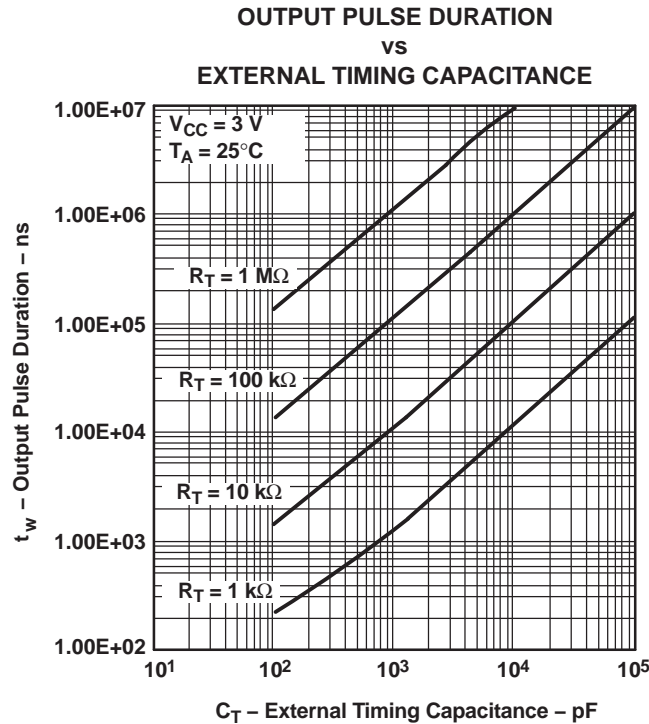


Figure 2.

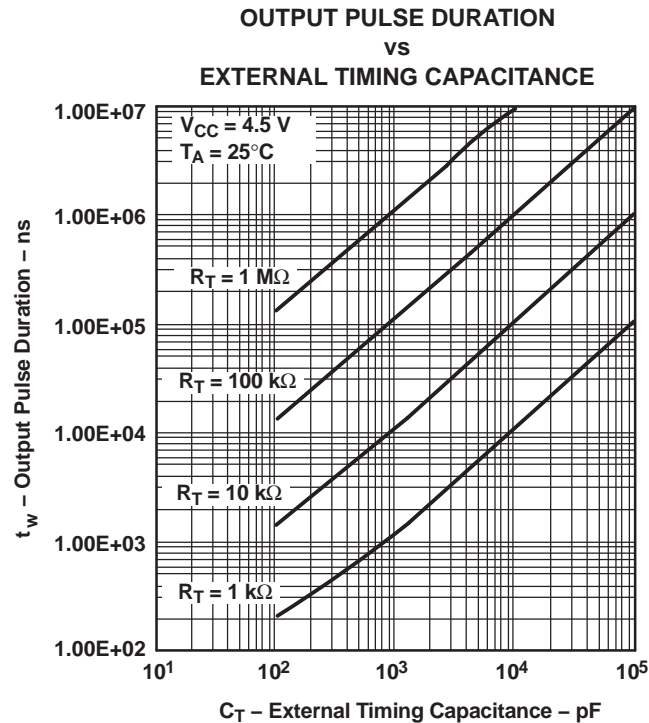


Figure 3.

APPLICATION INFORMATION

Operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied.

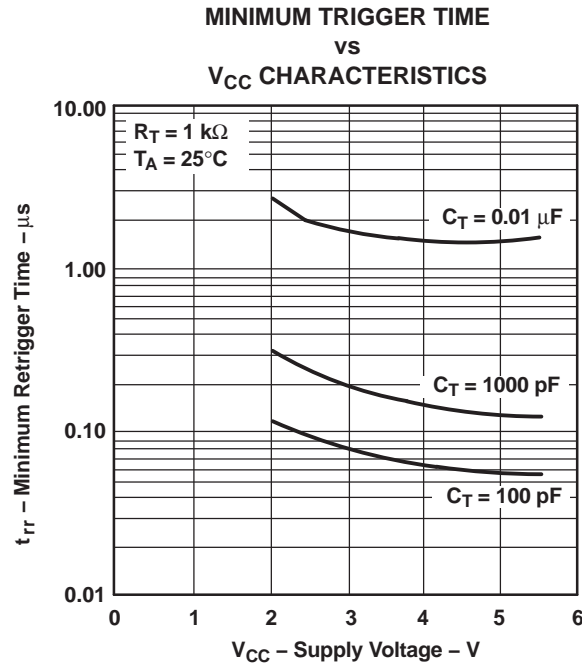


Figure 4.

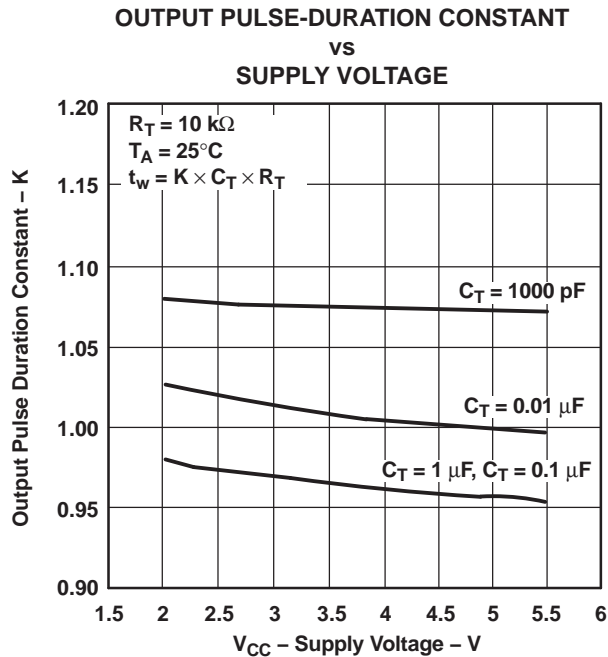


Figure 5.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74LV123ATPWRG4Q1	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV123ATPWRQ1	ACTIVE	TSSOP	PW	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN74LV123A-Q1 :

- Catalog: [SN74LV123A](#)
- Enhanced Product: [SN74LV123A-EP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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